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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/839,509
Filing Date: April 20, 2001
Appellant(s): STRUHSAKER ET AL.

Daniel E. Venglarik
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3-9-2006 appealing from the Office action mailed 5-3-2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US006091729A	DOVE	7-2000
US006760327B1	MANCHESTER	7-2004
US006560219B1	TABU	5-2003
US006512769B1	CHUI	1-2003
US005416776A	PANZARELLA ET AL.	5-1995
US005355090A	PAJOWSKI ET AL.	10-1994
US006047348A	LENTZ ET AL.	4-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 10-13, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Dove (U.S. 6,091,729).

Regarding Claim 10, Dove discloses for use in association with devices such as processor and modems used in wireless and wireline access systems (see FIG. 3, broadband fiber shelf 3), a backplane (see FIG. 4, backplane 305 and FIG. 5, cell buses 550) comprising: a higher tier that comprises one or more serial links (see FIG. 5, each cell bus/link 550 transmits cells serially, thus, each link/bus 550 is a serial link) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (see col. 4, lines 24-30; see col. 5, lines 16-20, 26-34, see col. 6, lines 10-19; see col. 7, line 4-65).

Regarding Claim 11, Dove discloses a higher tier bus (see FIG. 5, cell bus 550); and at least two switch matrix circuit boards (see FIG. 5, Two Cell Routing Unit CRU 220; see FIG. 3, Two CRU 220) coupled to said high tier bus (see col. 5, lines 41-35; see col. 7, lines 33-65). Regarding Claim 12, Dove discloses high speed serial links (see FIG. 2, plurality of cell bus links 550; and see FIG. 9, cell Bus A and B) coupled to said at least two switch matrix circuit board cads (see FIG. 2, CRU 220) and coupled to any other circuit board cards capable of sending and receiving high speed data traffic (see FIG. 2, OLU 230); see col. 6, lines 40-67; see col. 7, lines 5-32; see col. 10, lines 61 to col. 12, lines 12)

Regarding Claim 13, Dove discloses point-to-point serial links (see FIG. 9, cell Bus A and B) comprising differential pairs for both a transmit path and receive path (see col. 6, lines 30 to col. 7, lines 3; see col. 10, lines 61 to col. 12, lines 12; note that each link must have a transmit and receive pair).

Regarding Claim 17, Dove discloses at least two (2) high speed serial links (see FIG. 5, Cell clock 530 and cell sync 540; see FIG. 10, links between LIU 230 and ABIUs) for each interface control processor slot (see FIG. 5 and FIG. 2, AFIU 240) in said backplane (see col. 6, lines 5-67; see col. 5, lines 35-55; see col. 7, line 15-21,33-37; see col. 12, lines 12-30).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester (U.S. 6,760,327) in view of Tabu (U.S. 6,560,219).

Regarding Claim 1, Manchester discloses for use in association with devices such as processors and modems used in wireless and wireline access systems (see FIG. 2, Access Node 14), a backplane (see FIG. 3, Backplane 46) comprising:

a low tier that comprises a cell-based bus (see FIG. 3, TSB 70 that connects to ATM switch 66) capable of aggregate traffic rates of up to approximately a hundred megabit per second (see col. 8, lines 19-24; see col. 7, lines 45-65); and

a high tier that comprises one ore more serial links (see FIG. 3, HAS 72 bus contains one or more point-to-point serial links 76; see col. 8, lines 42-50) capable of aggregate traffic rates of up to approximately one gigabits per second (see col. 8, lines 19-25; see col. 7, lines 45-65).

Manchester does not explicitly disclose approximately two and twenty gigabits per second. However, Tabu teaches a low tier (see FIG. 7, cell switch 2100) aggregate traffic rates of up to approximately two gigabit per second (see col. 9, lines 65-67) and a high tier (see FIG. 7, cell switch 1100) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (see col. 9, lines 43-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide switches with approximately two gigabit per second and twenty gigabit per second, as taught by Tabu in the system of Manchester, so that it would provide a hybrid data exchange between different rates and systems, and accommodate in exchanging subscriber data between different rate switches; see Tabu col. 10, line 19-35, see col. 2, lines 60 to col. 3, lines 45.

Regarding Claim 2, Manchester discloses a low tier bus (see FIG. 3, TSB bus 70) comprising a switching architecture (see FIG. 3, switch core 44) that (1) allows a circuit board card on an input side of a connection (see FIG. 3, input of Line card 1) to transmit data to a circuit board card (see FIG. 3, Line card 2) on an output side of said connection (see FIG. 3, output from switch core 44), and that (2) allows a circuit board card on an output side of a connection (see FIG. 3, Line card 2) to receive data from a circuit board on the input side of said connection (see FIG. 3, receive output data from switch core 44; see col. 7, lines 39 to col. 8, lines 42).

Regarding Claim 3, Manchester discloses wherein said low tier bus supports one of packet based traffic, unicast traffic, multicast traffic, and broadcast traffic (see col. 8, lines 20-31, and see col. 6, lines 29-55). Tabu also discloses packet based traffic (see col. 10, lines 1-6).

Regarding Claim 4, Tabu discloses wherein said low tier bus supports asynchronous transfer mode traffic (see col. 10, lines 1-9). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide medium cell switch which process ATM traffic, as taught by Tabu in the system of Manchester, for the same motivation as described above in claim 1.

Regarding Claim 20, Manchester discloses a device (see FIG. 2, Access Node 14) comprising a backplane (see FIG. 3, Backplane 46) comprising:

a low tier that comprises a cell-based bus (see FIG. 3, TSB 70 that connects to ATM switch 66) capable of aggregate traffic rates of up to approximately a hundred megabit per second (see col. 8, lines 19-24; see col. 7, lines 45-65); and

a high tier that comprises one ore more serial links (see FIG. 3, HAS 72 bus contains one or more point-to-point serial links 76; see col. 8, lines 42-50) capable of aggregate traffic rates of up to approximately one gigabits per second (see col. 8, lines 19-25; see col. 7, lines 45-65) wherein said device comprises one of: an access process unit (see FIG. 29-30, Controller 652), a modem unit, and a combined access processor and modem unit (see col. 30, lines 25-35, see col. 31, lines 30-44).

Manchester does not explicitly disclose approximately two and twenty gigabits per second. However, Tabu teaches a low tier (see FIG. 7, cell switch 2100) aggregate traffic rates of up to approximately two gigabit per second (see col. 9, lines 65-67) and a high tier (see FIG. 7, cell switch 1100) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (see col. 9, lines 43-51), and access process unit (see FIG. 4, controller CC 150; see col. 7, lines 9-15). Therefore, it would have been obvious to one having ordinary skill in the art

at the time the invention was made to provide a switches with approximately two gigabit per second and twenty gigabit per second, as taught by Tabu in the system of Manchester, so that it would provide a hybrid data exchange between different rates and systems, and accommodate in exchanging subscriber data between different rate switches; see Tabu col. 10, line 19-35, see col. 2, lines 60 to col. 3, lines 45.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester in view of Tabu as applied to claims 1,2,4 above, and further in view of Chui (U.S. 6,512,769).

Regarding Claim 5, Manchester in view of Tabu discloses all of limitation as recited in claims 1,2,4 above.

Neither Manchester nor Tabu explicitly discloses wraps asynchronous transfer mode cells with a header to allow to switch cell based traffic according to the connection map. However, Chui discloses a lower tier bus (see FIG. 6, cell BUS) wraps asynchronous transfer mode cells with a header (see FIG. 9, ATM cell is encapsulated with cell bus header byte; see col. 8, lines 1-6) to allow to said lower tier bus to switch cell based traffic according to the connection map (see FIG. 24-25, connection address map RAM data) on each circuit board card (see FIG. 6; cards 606-608,610-612) connected to said low tier bus (see col. 5, lines 60 to col. 6, lines 67; see col. 8, line 47-58; see col. 14, lines 30-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to encapsulate the ATM cell into a cell bus frame in order to switch between the cards by utilizing the cell bus, as taught by Chui, in the combined system of Manchester and Tabu, so that it would provide fair rate-based cell traffic arbitration and provide

flexibility and a performance improvement in the translation of cell routing information; see Chui col. 2, lines 40-65.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester and Tabu as applied to claims 1,2,4 above, and further in view of Lentz (U.S. 6,047,348).

Regarding Claim 6, Manchester discloses said lower tier bus comprises two (2) parallel buses (see FIG. 3, 2 TSB buses). Neither Manchester nor Tabu explicitly discloses a thirty two (32) bit data path. However, a data bus having 32 bit data path is well known in the art. In particular, Lentz discloses a data bus having 32 bit data path (see FIG. 1, 32 bits data bus; see abstract, col. 2, lines 5-15; see col. 3, lines 10-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bit data bus, as taught by Lentz, in the combined system of Manchester and Tabu, so that it would provide a flexible frame word for low end products; see Lentz col. 2, line 5-40.

10. Claim 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester in view of Tabu.

Regarding Claim 7, Manchester discloses lower tier bus clock rate (see col. 8, lines 19-25; see col. 8, lines 50-65) equal to on half of a clock of said backplane (see col. 8, lines 19-50; see col. 9, lines 40-55, see col. 32, lines 45; it is inherent that low priority bus clock/data rate must be at least half of the clock/data rate of the entire backplane).

Regarding Claim 8, neither Manchester nor Tabu explicitly discloses clock rate 32.768 MHz. Manchester discloses a clock/data rate of 30 Mbps or 30 MHz. Setting clock rate to 32.768 MHz does not define a patentable distinct invention over that in the combined system of

Manchester and Tabu, since both the invention as a whole and the combined system of Manchester and Tabu are directed to setting low clock/data rate for low speed traffic and setting high clock/data rate for high speed traffic. The degree in which determining clock rate presents no new or unexpected results, so long as the low and high-speed traffic is switched via appropriate buses. If one has less clock rate, it will be used for low speed traffic, and if one has number clock rate, it will be used for high speed traffic. Therefore, to have clock rate of 32.768 that at low speed bus would have been routine experimentation and optimization in the absence of criticality.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester and Tabu, as applied to claim 1 and 2 above, and further in view of Pajowski (U.S. 5,355,090).

Regarding Claim 9, Neither Manchester nor Tabu explicitly discloses a redundant clock reference. However, having a redundant clock reference is well known in the art. Pajowski discloses a redundant clock reference (see FIG. 1, see abstract; col. 2, lines 44-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a redundant clock system, as taught by Pajowski, in the combined system of Manchester and Tabu, so that it would over timing problems by reducing timing errors; see Pajowski col. 2, line 5-40.

12. Claim 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove.

Regarding Claim 14, Dove discloses high speed serial links operate at a clock rate equal to a clock of said backplane (see col. 4, lines 20-30; see col. 5, lines 15-35).

Regarding Claim 15, Dove does not explicitly discloses clock rate 65.536 MHz. Dove discloses a clock rate of 100 MHz. Setting clock rate to 65.536 MHz does not define a patentable

distinct invention over that in the system of Dove, since both the invention as a whole and the system of Dove is directed to setting maximum cell bus clock rate to 100 MHz in order to support aggregate bandwidth of switching fabric of up to 20Gbps. The degree in which determining clock rate presents no new or unexpected results, so long as the traffic can be switched up to 20Gbps. Therefore, to set clock rate of 65.536 MHz would have been routine experimentation and optimization in the absence of criticality.

Regarding Claim 16, Dove discloses a high speed serial link serial/de-serial device (see FIG. 5, CRU 220), high speed serial link bit encoding (see FIG. 5, CRU 220 and OLU 510; see col. 7, line 5-31; see col. 2, line 30-31; X bits) and high speed serial link clock rate (see col. 8, lines 19-41) as described above in claims 10-14. Dove does not explicitly disclose multiplying the clock rate by a factor of twenty and a link encoding 8Bit/10Bit. Multiplying the clock rate by 20 and setting ending to 8B/10B does not define a patentable distinct invention over that in the system of Dove, since the invention as a whole and the system of Dove is directed to meet the functional needs of the switch. The degree in which multiplying clock rate by twenty and setting encoding to 8B/10B presents no new or unexpected results, so long as the switch can perform and meet its functional needs. Therefore, to multiply the clock rate by twenty and setting the encoding 8B/10B would have been routine experimentation and optimization in the absence of criticality.

13. Claim 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manchester and Tabu, as applied to claim 1 and 2 above, and further in view of Panzarella (U.S. 5,416,776).

Regarding Claim 18, neither Manchester nor Tabu explicitly disclose one of a time division multiplex bus, a communication bus, a communication bus, a common control bus, and a joint Test Access Group test bus. However, implementing a common/control bus in the backplane is well known in the art. In particular, Panzarella discloses one of a time division multiplex bus (see FIG. 1, TDM bus 201) and/or a common control bus (see FIG. 1, Management bus 401) (see col. 3, lines 60 to col. 4, lines 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a backplane with common control bus and TDM bus, as taught by Panzarella, in the combined system of Manchester and Tabu, so that it would provide a backplane which capable of enabling high speed network communication among larger number of modems and related circuits and increasing the number of buses which offers distinct advantages for chassis requiring a substantial number of modems and related circuit boards; see Panzarella col. 1, line 20 to col. 2, lines 4.

Regarding Claim 19, Manchester discloses at least one set of clock and framing resources (see FIG. 2, line slots 56 and switch slots 54; see FIG. 3, input to ATM switch 66; see col. 7, lines 16-56; see col. 8, lines 5-50). Panzarella discloses at least one set of clock and framing resources (see col. 3, lines 5-14, 45-67 and see col. 4, lines 14-30).

(10) Response to Argument

1. **Regarding claims 10-13 and 17, the applicant argued that**, "...**a.** The recited serial link(s) are not found in the cited reference...Dove does not use the term "serial" anywhere..." in the page 6, section 1.a. and page 7, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with argument above. Dove discloses one or more serial links (see FIG. 5, **each cell bus/link 550 transmits cells serially between one end point CBI_1 520 to another end point $CBI_{(1)}$ 510, thus, each link/bus 550 is a point-to-point serial link, and there are "n" link/bus 550**) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (**see col. 4, lines 24-30; see col. 5, lines 16-20, 26-34, see col. 6, lines 10-19; see col. 7, line 4-65**).

Also, it is clear to one skilled in the ordinary art that very basic and fundamental concept of transmitting data (**see Dove FIG. 5, data**) from one end point (**see Dove FIG. 5, CBI_1 520**) to the other end point (**see Dove FIG. 5, $CBI_{(1)}$ 510**) over a signal link/bus (**see Dove FIG. 5, a link/bus 550**), the data must be send in **serial, sequential order, or one after another** (see Dove FIG. 5 below). Thus, Dove's link/bus 550 is a serial link/bus that performs data transmission in serial, sequential order, or point-to-point since there is no other way to send data in a point-to-point connection with a single link/bus. Again, Dove discloses the "functionality" of "serial" transmission by showing a single link/bus 550 that connects between two points and performs serial/sequential transmission since one skill in the ordinary art would clearly understand well established basic point-to-point transmission concept where data must be send in serial or sequential order.

Regarding claims 10-13 and 17, the applicant argued that, "... such an interpretation of "serial link" is contrary to the ordinary and accepted meaning of the term...The interpretation is also inconsistent with the specification of the subject application ...Because the specification as filed compels an interpretation of "serial link" as excluding cell-based buses such as cell bus 450 in Dove, the interpretation asserted in the final rejection cannot be accepted...The

interpretation is also inconsistent with ordinary usage of the term. U.S. Patent No. 6,760,327 to Manchester et al, for example, specifies that serial link 76 includes a single data signal...The cell bus 450 in Dove transmits cells (53 bytes) of data concurrently, Not bitwise, and therefore does NOT comprise a "serial link..." in section 1.a. and page 7-8.

In response to applicant's argument, the examiner respectfully disagrees with argument above. First, neither in the office action nor Dove recites a cell bus **450**. Thus, applicant argument on bus 450 is ambiguous and unclear.

Second, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (**i.e., excluding cell-based buses, bitwise, or cells (53 bytes) of data concurrently**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, it is irrelevant to argue the limitation that is not being claimed.

Third, examiner's interpretation of "serial link" neither contrary to specification nor ordinary and accepted meaning of the term since both applicant's serial bus/link 415 (see applicant FIG. 4) and Dove's serial link/bus 550 (see Dove's FIG. 5) are identical and performed identical functionality as shown below.

Applicant's FIG. 4

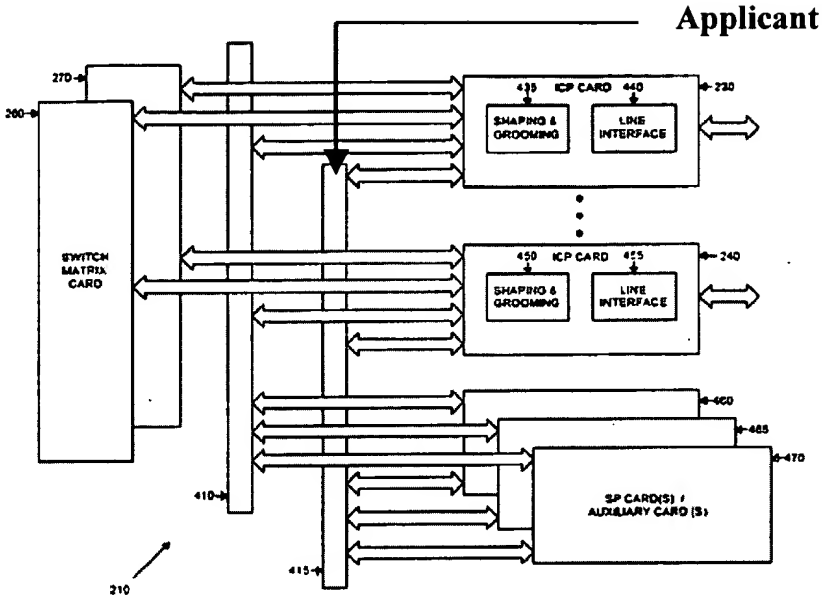


FIGURE 4

Dove's FIG. 5

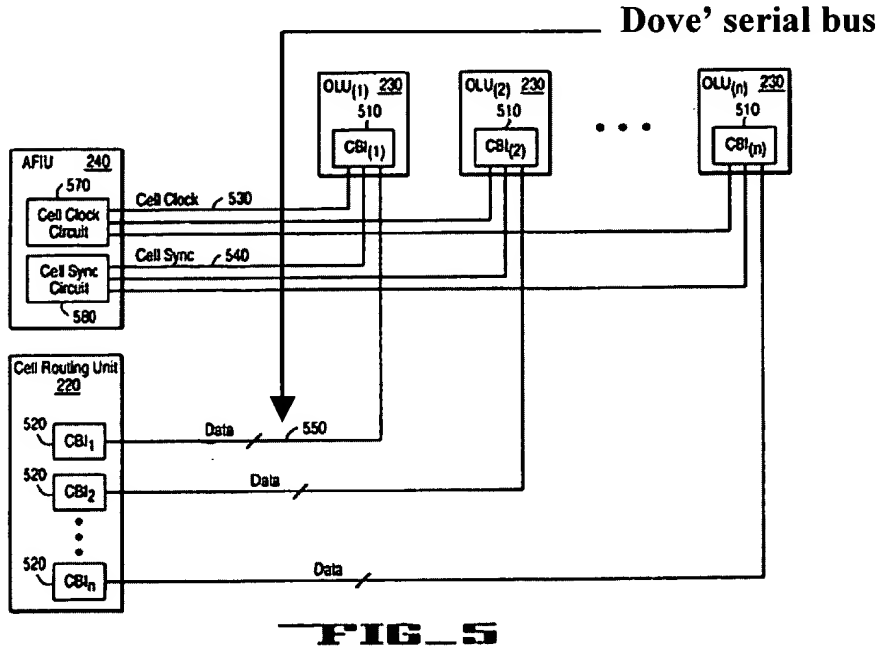


FIG_5

Fourth, Dove also discloses one or more point-to-point or serial link/bus 550 in col. 7, line 33-36,55-56 as set forth below.

The cell bus of FIG. 5 supports a direct **point to point link** between the ATM switching fabric of the CRU 220 (FIG. 2) and each OLU 230. Within each cell bus frame, a complete ATM cell (53 bytes) is transferred across the cell bus.

As discussed above, **the data lines 550 are wired point to point from the CRU 220 to each OLU 230**. (Emphasis added).

Fourth, regarding argument on Manchester, it is irrelevant since Manchester is not being used to reject the argued claim limitation. By having a serial link is notoriously well established in the art as one can evident from the response above, and accordingly examiner's interpretation of a serial link is clearly consistent with applicant's specification/drawing and ordinary and accepted meaning of the term.

Thus, it is clear that Dove's serial bus/link 550 clearly anticipates the applicant's "serial bus/link".

Regarding claim 17, the applicant argued that, "...claim 17 recites the backplane comprises at least two high speed serial links for each interface control processor slot in the backplane. Such a feature is not found in the cited reference...Dove depicts only a single cell bus, not multiple serial links for each interface control processor slot as recited in the claim" in page 8, section 1.b and page 10, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees with the argument above. Dove discloses at least two (2) high speed serial links (**see FIG. 5, Cell clock 530 and cell sync 540 between AFIU 240 and OLU 230; see FIG. 10, links between LIU 230 and ABIUs**) for each interface control processor slot (**see FIG. 5 and FIG. 2, AFIU 240**) in said backplane (**see col. 6, lines 5-67; see col. 5, lines 35-55; see col. 12, lines 12-30; see col. 7, line 15-21,33-37**) as shown below.

Dove's FIG. 5

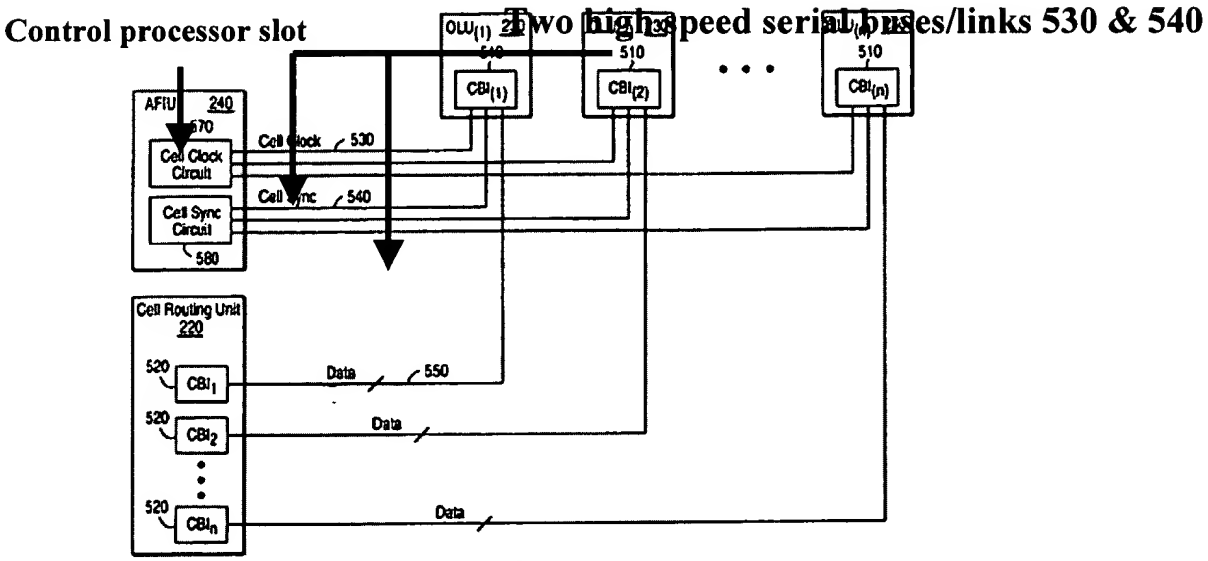


FIG_5

Dove discloses high speed serial cell clock 530 bus/link and cell sync 540 bus/link at AFIU 240 (ATM Fiber Bank Interface Unit) as recited in col. 7, line 15-21,33-37. As set forth above, examiner is clearly asserting and reciting that a cell clock 530 link/bus and cell synch 540 links, not a single cell bus 500 argued by the applicant, anticipate applicant's "at lest two high speed serial links for each interface processor slot".

2. **Regarding claims 1-4, 7-8 and 20, the applicant argued that**, "...independent claims 1 and 20 each cites that the low tier comprises a cell-based bus capably of lower aggregate traffic rates (up to approximately two gigabits per second), while the high tier comprises one or more serial links capable of higher aggregate traffic rates (up to approximately twenty gigabits per second). Such a feature is not found in the cited references...The structure disclosed in Manchester is thus precisely the opposite of the structure that is recited in the claims: the cell-

based bus 72 in Manchester provides a high speed connection rather than a lower speed connection as required in the claims for the recited cell-based bus, while the serial bus 70 in Manchester provides a slower connection than bus 72 rather than the higher speed connection as required for the serial links recited in the claims..." in the page 10, section 2; page 11, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees with argument above. Manchester discloses a low tier that comprises a cell-based bus (**see FIG. 3, TSB 70 that connects to ATM switch 66**) capable of aggregate traffic rates of up to approximately a hundred megabit per second (**see col. 8, lines 19-24; see col. 7, lines 45-65**); and

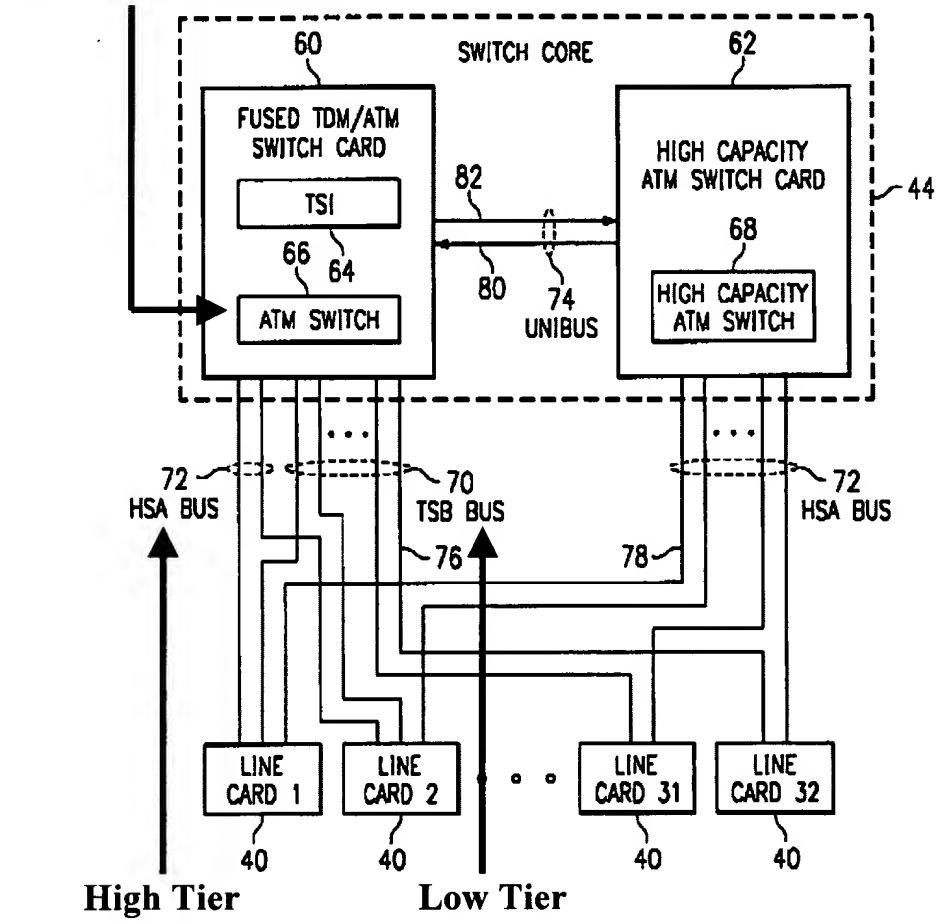
a high tier that comprises one ore more serial links (**see FIG. 3, HAS 72 bus contains one or more point-to-point serial links 76; see col. 8, lines 42-50**) capable of aggregate traffic rates of up to approximately one gigabits per second (**see col. 8, lines 19-25; see col. 7, lines 45-65**).

Tabu teaches a low tier (**see FIG. 7, cell switch 2100**) aggregate traffic rates of up to approximately two gigabit per second (**see col. 9, lines 65-67**) and a high tier (**see FIG. 7, cell switch 1100**) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (**see col. 9, lines 43-54**).

Thus, it is clear that the combined system of Manchester and Tabu disclose the claimed invention.

Moreover, Manchester TSB bus 70 is a point-to-point ATM "**cell-based**" bus since it is connected to ATM cell switch 66 as shown in FIG. 3 below.

FIG. 3



Manchester discloses a point-to-point ATM "cell-based" switching (via ATM switch 66) in TSB bus 70 as described in col. 8, line 5-12,43-46,52-54 below.

"...Referring to FIG. 3, the switch core 44 includes a fused TDM/ATM switch card 60 and a high capacity ATM switch card 62. The fused TDM/ATM switch card 60 includes a time slot interchanger (TSI) 64 and **a multi-purpose ATM switch 66** that are together capable of switching both synchronous and asynchronous traffic... the **TSB bus 70 comprises a full-duplex, point-to-point serial link** 76 between each line card 40 and the fused TDM/ATM switch card 60... **Each point-to-point serial link** 76 of the TSB bus 70 includes a single data signal to minimize pin usage, a frame indicator signal, and an associated clock signal in each direction..." (Emphasis added)

Manchester also discloses a point-to-point or **serial** switching in HAS bus 72 as shown above and recited in col. 8, line 66 to col. 9, line 4 below.

"...the ATM bus 72 comprises a high-speed ATM (HSA) bus. The HSA bus 72 comprises a full-duplex, **point-to-point link** 78 between each line card 40 and the high capacity ATM switch card 62. **The point-to-point bus** configuration provides signal robustness ..." (Emphasis added)

Thus, it is clear that Manchester discloses precisely and clearly applicant's claimed and argued invention of "cell-based" tier and "serial tier" buses/links.

Regarding claims 1-4, 7-8 and 20, the applicant argued that, "...Tabu contains no teaching of any of the switches 1100, 2100 and 3100 including both a cell bus and a serial link, or of a serial link supporting a 2Gbps data rate in addition to switches 1100,2100 and 3100. Neither Manchester nor Tabu provides any motivation or incentive for modifying the teaching of Manchester to implement a lower speed cell bus and a high speed serial link rather than vice versa" in the section 2, page 11, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees with argument above.

Claim 1, recites, "a lower tier that comprises a cell-based bus **capable of** aggregate traffic rates **up to approximately** two gigabits per second; and

A higher tier that comprises one or more serial links **capable of** aggregate traffic rates of **up to approximately** twenty gigabits per second". (Emphasis added).

The term "**capable of...**" indicates "having ability" or "having capability". Thus, it is clear that the limitations that follow "capable of" are **optional**. A bus/tier is capable of aggregating traffic rates up to approximately two Gbps, and it means that a bus/tier may or may not aggregating traffic rates up to approximately two Gbps.

Manchester already discloses a low tier that comprises a cell-based bus (see FIG. 3, TSB 70 that connects to ATM switch 66) **capable of** aggregate traffic rates of up to approximately **a hundred megabit per second** **(see col. 8, lines 19-24; see col. 7, lines 45-65)**; and

a high tier that comprises one ore more serial links (see FIG. 3, HAS 72 bus contains one or more point-to-point serial links 76; see col. 8, lines 42-50) **capable of** aggregate traffic rates of up to approximately **one gigabits per second** (see col. 8, lines 19-25; see col. 7, lines 45-65).

Thus, secondary reference (Tabu) is not even require since it would have been so obvious to one having ordinary skill in the art at the time the invention was made to increase the low tier rate from 100 megabit per second to approximately 2 gigabit per second and a higher tier from 100 megabit/one gigabit per second to twenty gigabit per second so that it would provide faster data transmission on the bus.

Examiner, although it is not needed, supplies a secondary reference (Tabu) to show the well-known and obvious optional claimed limitation. Manchester clearly and precisely discloses a cell bus and a serial link, and Tabu further discloses a lower tire with 2 Gbps data rate as set forth above. Thus the combined system of Manchester and Tabu disclosed the argued claim invention.

Regarding argument on lack of motivation to **implement a lower speed bus and a high speed serial link**, examiner does not required to provide any motivation to implement buses for the following reasons:

a) The a cell-base lower bus and a point-to-point serial bus are clearly disclosed by the primary reference Manchester as set forth above.

b) The examiner neither recite nor suggest to implement a lower speed bus and a high speed serial link in view of Tabu teaching.

c) One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the rejection is based in the combined system of Manchester and Tabu as set forth above.

Moreover, examiner has already provided a motivation to **implement switches/tiers with approximately two gigabit per second and twenty gigabit per second** as taught by Tabu since the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide switches with approximately two gigabit per second and twenty gigabit per second, as taught by Tabu in the system of Manchester, so that it would provide a hybrid data exchange between different rates and systems, and accommodate in exchanging subscriber data between different rate switches; see Tabu col. 10, line 19-35, see col. 2, lines 60 to col. 3, lines 45.

3. **Regarding claim 5, the applicant argued that,** "...ATM cells are wrapped with a header to allow board switching based on a connection map...the cited portion of Chui does not...teach that the header depicted in Figure 9 therein is used for circuit board level switching of ATM cells, but instead teaches precisely the opposite..." in the page 12, section 3.

In response to applicant's argument, the examiner respectfully disagrees with argument above. Chui discloses a lower tier bus (**see FIG. 6, cell BUS**) wraps asynchronous transfer mode cells with a header (**see FIG. 9, ATM cell is encapsulated with cell bus header byte; see col. 8, lines 1-6**) to allow to said lower tier bus to switch cell based traffic according to the connection map (**see FIG. 24-25, connection address map RAM data; or see FIG. 14, RAM 1416**) on each circuit board card (**see FIG. 6; cards 606-608,610-612**) connected to said low tier bus (**see col. 5, lines 60 to col. 6, lines 67; see col. 8, line 47-58; see col. 14, lines 30-65**).

Chui's FIG. 9 discloses a cell format (which utilizes by cell bus in FIG. 6) comprising a cell bus header which wraps/encapsulates ATM cells. Moreover, a cell format (defined in FIG. 9) is switched in the cell bus according to address map RAM look-up logic in order to determine where the target/destination service modules and perform switching accordingly. Chui discloses in col. 8, lines 43-44, 48-53:

"For ATM traffic....**the ECP performs cell bus interface polling address to target address mapping** using thirty-two possible polling address destinations that are mapped to twenty-six targets. **The mapping is performed by Address Map RAM 1416 look-up logic**, wherein the targets are the service modules via a CBM, a second PSM Card via a CBS, and a MCE..." (Emphasis added)

Thus, it is clear that Chui discloses the target/destination address map lookup is performed for ATM encapsulated bus cell format (defined in FIG. 9) switching.

Regarding the argument on claim 1 under section 3, please see responses in section 2 above.

4. **Regarding claim 6, the applicant argued that**, "...two parallel buses each having a 32-bit data path. Such a feature is not found in the cited reference...no specific motivation or incentive to employing (two) 32 bit data paths in lower tier..." in the page 13, section 4.

In response to applicant's argument, the examiner respectfully disagrees with argument above. Note that a data bus having 32 bit data path is well known and established in the art. In particular, Lentz discloses a data bus having 32 bit data path (**see FIG. 1, 32 bits data bus; see abstract, col. 2, lines 5-15; see col. 3, lines 10-15**).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bit data bus, as taught by Lentz, in the combined system of Manchester and Tabu, so that it would provide a flexible frame word for low end products; see Lentz col. 2, line 5-40.

Regarding the argument on claim 1 under section 4, please see responses in section 2 above.

5. **Regarding claim 9, the applicant argued that,** "...providing a redundant clock reference for the lower tier. Such a feature is not found in the cited reference. Nothing in either over Manchester or Tabu suggests that timing error in (asynchronous) ATM buses of the type disclosed therein are such a problem as to motivate one skilled in the art to look to clock redundancy for synchronous system as described in Pajowski..." in the page 13, section 5.

In response to applicant's argument, the examiner respectfully disagrees with argument above. Pajowski discloses a redundant clock reference (see FIG. 1, see abstract; col. 2, lines 44-65).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a redundant clock system, as taught by Pajowski, in the combined system of Manchester and Tabu, so that it would over timing problems by reducing timing errors; see Pajowski col. 2, line 5-40.

Regarding argument on "asynchrous" vs. "synchronous", it is well established in the art that "ATM" utilizes "**asynchrous transmission**", and it does **not** mean that **every ATM system uses "asynchrous clocking", "no clocking", or "no synchronization**". One cannot

assume due to the fact that ATM system performs asynchrous "transmission", and thus it has no clocking or synchronizing. Manchester also discloses the use of Synchronous Optical Network (SONET), which utilizes "clocking/synchronization" in conjunction with ATM system (see col. 6, line 15-22). Tabu also discloses the use of STM (Synchronous Transfer Mode) and ATM (see col. 3, line 43-65). Moreover, ATM cells are transported over Synchronous Optical Network (SONET) that utilizes "clocking" or "synchronization" (**see EXHIBIT A**, GR-2837-CORE, sections 4 and 4; and **see EXHIBIT B**, GR-253-CORE, sections 3 and 5).

One skill in the art would clearly look into clock redundancy in order to improve the "clocking/synchronization" of asynchronous (ATM) transmission. Thus, it would have been to one having ordinary skill in the art at the time the invention was made to provide a redundant clock system, as taught by Pajowski, in the combined system of Manchester and Tabu for the motivation as set forth above.

Regarding the argument on claim 1 under section 5, please see responses in section 2 above.

6. **Regarding claims 14-16, the applicant argued that**, "...claim 14 recites that the serial links operable at the same clock rates as the back plane. Such a feature is not found in the cited reference. The portions of Dove cited in the final rejection state that the cell bus is clocked at 100 MHz, but are silent as to the clocking rate of either the serial links or the back plane...claim 15 recites that the high speed serial link clock rate is 65.536 MHz. Claim 16 recites that the high speed serial link serialization/deserialization devices multiply the link clock rate by a factor of 20

and wherein each speed serial link is 8B/10B encode...such reasoning fails to establish...obviousness" in the page 14, section 6.

In response to applicant's argument, the examiner respectfully disagrees with argument above.

Regarding Claim 14, Dove discloses high speed serial links operate at a clock rate equal to a clock of said backplane (**see col. 4, lines 20-30; see col. 5, lines 15-35; 100 MHz**). Note that a cell bus 500 comprises "n" serial links/buses 550 as shown in FIG. 5, and thus examiner asserts "serial links" as "n" serial links/buses 550 (i.e. a cell bus 500). As set forth in FIG. 4, a backplane is coupled to a cell bus 500 (see col. 6, line 40 to col. 7, line 4). Thus, it is obvious that "n" serial links/buses 550 (i.e. a cell bus 500) and a backplane must operate at the same clock rate of "100 MHz" in order to support an aggregate bandwidth of a switching fabric of up to 20 Gbps (see Dove col. 4, line 20-30).

Regarding Claim 15, Dove discloses a clock rate of 100 MHz as set forth in claim 14 above. Setting clock rate to 65.536 MHz does not define a patentable distinct invention over that in the system of Dove, since both the invention as a whole and the system of Dove is directed to setting maximum cell bus clock rate to 100 MHz in order to support aggregate bandwidth of switching fabric of up to 20Gbps. The degree in which determining clock rate presents no new or unexpected results, so long as the traffic can be switched up to 20Gbps. Therefore, to set clock rate of 65.536 MHz would have been routine experimentation and optimization in the absence of criticality. Note that **none** of the applicant disclosure recites **the benefit of new or unexpected result of** setting a clock rate to 65.536 MHz. In fact, the clock can be set to any rate so long as it can support the aggregate bandwidth of switching per Dove (see col. 4, line 20-30).

Regarding Claim 16, Dove discloses a high speed serial link serial/de-serial device (**see FIG. 5, CRU 220**), high speed serial link bit encoding (**see FIG. 5, CRU 220 and OLU 510; see col. 7, line 5-31; see col. 2, line 30-31; "X" bits**) and high speed serial link clock rate (**see col. 8, lines 19-41**) as described above in claims 10-14. Dove does not explicitly disclose multiplying the clock rate by a factor of twenty and a link encoding 8Bit/10Bit. However, Multiplying the clock rate by 20 and setting ending to 8B/10B does not define a patentable distinct invention over that in the system of Dove, since the invention as a whole and the system of Dove is directed to meet the functional needs of the switch. The degree in which multiplying clock rate by twenty and setting encoding to 8B/10B presents no new or unexpected results, so long as the switch can perform and meet its functional needs. Therefore, to multiply the clock rate by twenty and setting the encoding 8B/10B would have been routine experimentation and optimization in the absence of criticality. Note that **none** of the applicant disclosure recites **the benefit of new or unexpected result of** multiplying the clock rate by a factor of twenty. In fact, the clock can be set to any rate by multiplying an original rate with any factor in order obtain the rate which can support the aggregate bandwidth of switching per Dove (see Dove col. 4, line 20-30). Likewise, **none** of the applicant disclosure recites **the benefit of new or unexpected result of** a link encoding 8Bit/10Bit. Dove discloses a cell bus encoding a cell bus frame of "X" bits in length (see col. 2, line 30-31). Thus, it would have been obvious to use 8 bit input is encoded into 10 bit output encoding in order to achieve the "X" bits cell frame of Dove.

Regarding the argument on claim 10 under section 5, please see responses in section 1 above.

7. **Regarding claims 18-19, the applicant argued that,** "...claim 18 recites providing a time division multiplex bus, a communication bus, a common control bus **and/or** a Joint test Access Group bus on the backplane. Such a feature is not found in the cited reference. Panzarella ...does not suggest the specific buses recited in the claims or incorporating such buses for a particular purpose" in the page 14, section 6.

In response to applicant's argument, the examiner respectfully disagrees with argument above. First, claim 18 recites, "further comprising one of:" Thus, examiner is only require to show only "**one**" limitation or "one' type of bus, not all the buses. In particular, Panzarella discloses one of a time division multiplex bus (**see FIG. 1, TDM bus 201**) and/or a common control bus (**see FIG. 1, Management bus 401);** see col. 3, lines 60 to col. 4, lines 4. Moreover, Panzarella does not require to discloses "incorporating such buses for a particular purpose" since such limitation is not being claimed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding the argument on claim 1 under section 7, please see responses in section 2 above.

Attachments

EXHIBIT A: GR-2837-CORE

EXHIBIT B: GR-253-CORE

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ian N. More
June 1, 2006

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Section 6.2.1 contains the criteria for DS3 and STS-1 path maintenance signals (see Figure 6-5).

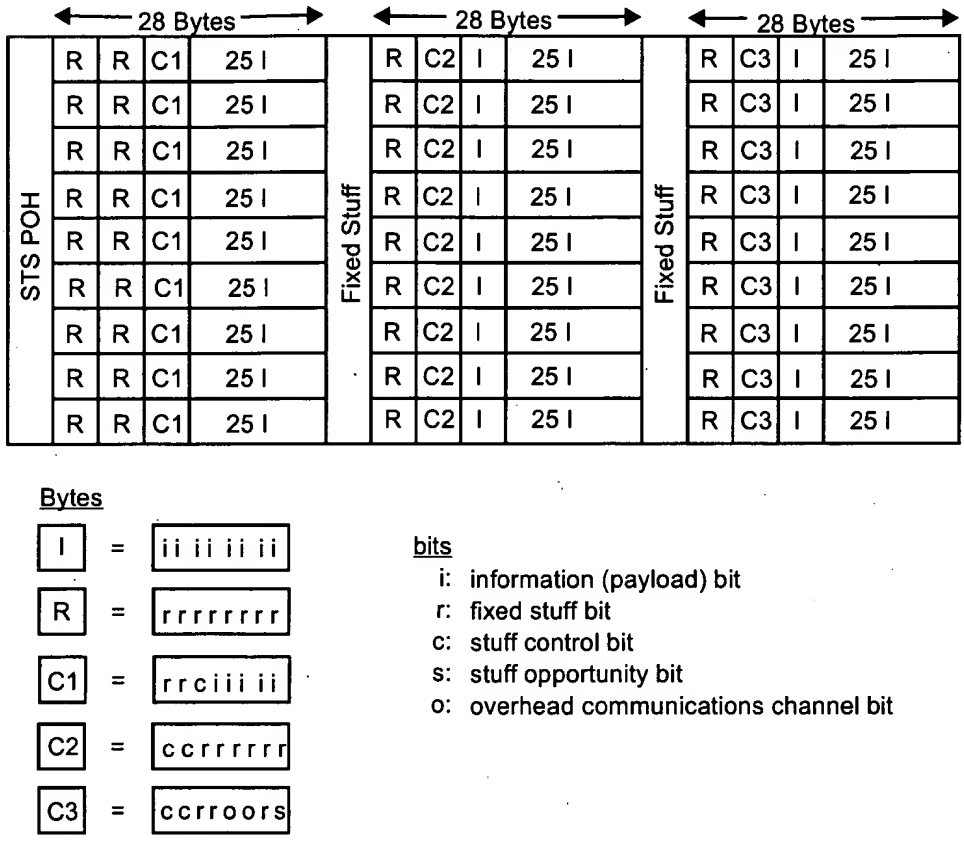

Figure 3-32. Asynchronous Mapping for DS3 Payload

3.4.2.2 Asynchronous Transfer Mode (ATM) Mapping for B-ISDN Applications

A method for mapping ATM cells (each of which consists of a 5-byte cell header and a 48-byte payload) into the payload capacity of an STS-1 SPE is defined. If this mapping is supported, then the following requirement is applicable.

R3-75 **[72]** ATM cells shall be mapped into the STS-1 Payload Capacity by aligning the byte structure of every cell with the byte structure of the STS-1 SPE. The entire STS-1 Payload Capacity (i.e., 84 columns) shall be filled with cells, yielding a transfer capacity for ATM cells of 48.384 Mb/s.

Because the STS-1 Payload Capacity is not an integer multiple of the 53-byte ATM cell length, some cells will cross an SPE boundary.

3.4.3.1.3 *Asynchronous Transfer Mode (ATM) Mapping for B-ISDN Applications*

A method for mapping ATM cells (each of which consists of a 5-byte cell header and a 48-byte payload) into the payload capacity of an STS-3c SPE is defined in this section. If this mapping is supported, then the following requirement is applicable.

R3-84 **[79]** ATM cells shall be mapped into the STS-3c Payload Capacity by aligning the byte structure of every cell with the byte structure of the STS-3c SPE. The entire STS-3c Payload Capacity (i.e., 260 columns) shall be filled with cells, yielding a transfer capacity for ATM cells of 149.760 Mb/s.

Because the STS-3c Payload Capacity is not an integer multiple of the 53-byte ATM cell length, some cells will cross an SPE boundary.

Cell payload scrambling is used to provide security against payload information replicating the (for example) frame synchronous scrambling sequence used at the SONET Section layer. Details of the cell payload scrambler are contained in TR-NWT-001112.

3.4.3.1.4 *DQDB Metropolitan Area Network (MAN) Mapping*

A mapping for DQDB into an STS-3c SPE is defined in this section. In this mapping, DQDB layer slots are transported in the payload capacity of an STS-3c SPE. In addition, the mapping uses three of the STS POH bytes, as follows:

- The F2 (User Channel) and Z3 (Growth) bytes are used to carry the DQDB Layer Management (M1 and M2) bytes.
- Bits 1 and 2 of the H4 (Indicator) byte are used to carry the Link Status Signal (LSS).
- Bits 3 through 8 of the H4 byte are used to indicate the offset from the H4 byte to the beginning of the next 53-byte DQDB slot.

If the DQDB mapping is supported, then the following criteria apply.

R3-85 **[80]** DQDB slots shall be mapped into the STS-3c Payload Capacity by aligning the byte structure of every slot with the byte structure of the STS-3c SPE. The entire STS-3c Payload Capacity (i.e., 260 columns) shall be filled with slots, yielding a transfer capacity for DQDB slots of 149.760 Mb/s.

R3-86 **[81]** Bits 3 through 8 of the H4 byte shall contain a binary number in the range from '000000' (0) to '110100' (52) that indicates the offset between the H4 byte and the boundary of the first DQDB slot following the H4 byte.

3.4.3.1.5 HDLC-Over-SONET Mapping

As noted in Section 3.4.2.3, the HDLC-over-SONET mapping described in that section can also be used for the transport of HDLC-framed signals in STS-3c SPEs. If such a mapping is supported, the criteria in Section 3.4.2.3 apply, with "STS-1" replaced by "STS-3c".

As was the case for the STS-1 HDLC-over-SONET mapping, the entire STS-3c Payload Capacity (i.e., 260 columns) is filled with HDLC frames and HDLC flags (as necessary). This results in a maximum transfer capacity of 149.760 Mb/s for HDLC-framed signals carried in a nominal rate STS-3c SPE.

3.4.3.2 Mappings into STS-12c SPEs

The STS-12c SPE is a 1044-column by 9-row structure. The first column contains the STS POH bytes. In all of the currently defined mapping, the STS POH is followed by three columns of fixed stuff bytes, and the remaining 1040 columns are the STS-12c Payload Capacity.

3.4.3.2.1 Asynchronous Transfer Mode (ATM) Mapping for B-ISDN Applications

A method for mapping ATM cells (each of which consists of a 5-byte cell header and a 48-byte payload) into the payload capacity of an STS-12c SPE is defined in this section. If this mapping is supported, then the following requirement is applicable.

R3-89 **[84]** ATM cells shall be mapped into the STS-12c Payload Capacity by aligning the byte structure of every cell with the byte structure of the STS-12c SPE. The entire STS-12c Payload Capacity (i.e., 1040 columns) shall be filled with cells, yielding a transfer capacity for ATM cells of 599.040 Mb/s.

Because the STS-12c Payload Capacity is not an integer multiple of the 53-byte ATM cell length, some cells will cross an SPE boundary.

Cell payload scrambling is used to provide security against payload information replicating (for example) the frame synchronous scrambling sequence used at the SONET Section layer. Details of the cell payload scrambler are contained in TR-NWT-001112.

3.4.3.2.2 HDLC-Over-SONET Mapping

As noted in Section 3.4.2.3, the HDLC-over-SONET mapping described in that section can also be used for the transport of HDLC-framed signals in STS-12c SPEs.

5. Network Element Architectural Features

This section describes various architectural features required in SONET NEs, particularly:

- Multiplexing procedures
- Overhead function usage
- Automatic Protection Switching (APS)
- Network synchronization
- Framing
- Jitter and wander performance.

5.1 Multiplex Procedures

5.1.1 Interleaving

An STS-N module either can be created directly (e.g., by the equipment that creates an STS-12 and maps ATM traffic into the STS-12c SPE), or it can be formed by byte-interleaving lower-level modules (e.g., STS-1s and STS-Ms). For STS-Ns that are formed by byte-interleaving lower-level modules, the following requirements are applicable:

R5-1 **[131]** Before byte-interleaving to form an STS-N, the transport overhead byte positions of all the constituent STS-1s and STS-Ms shall be frame aligned.

The alignment of the STS-1s and STS-Ms is accomplished by adjusting the STS Payload Pointers to reflect the new relative positions of the STS SPEs.[1]

Note that in development of these requirements, it is useful to assume that an NE that forms an STS-N (N > 3) will first logically interleave any STS-1 inputs (in sets of three consecutive STS-1s) to form STS-3 modules, and then interleave those STS-3 modules and any other STS-M inputs to form the STS-N. However, there are no requirements concerning the internal architectures of SONET NEs (e.g., an NE

1. In the SONET interface layer model described in Section 3.3, it would be the responsibility of the Line layer to align and interleave the signals that it receives from the Path layer. These criteria are written based on the assumption that the NE uses Path and Line layer signals that contain all of the Transport Overhead byte positions (e.g., that an internal path layer signal carrying an STS-1 SPE has a nominal bit rate of 51.84 Mb/s); however as discussed in Section 3.3, there are no criteria concerning the internal signals used by an NE. If the NE uses some other type of internal signals, then it must perform an equivalent process so that the structure of the interface signals (i.e., the OC-N or STS-N electrical signals transmitted by the NE) is independent of the type of internal signals used.

5.1.2 Concatenation

In all of the uses of STS-Nc SPEs currently defined in SONET, the STS-Nc SPE contains a single payload mapping (e.g., the ATM mapping into an STS-12c SPE described in Section 3.4.3.2.1), and therefore it is created in a single STS PTE. If future uses are defined that require an STS-Nc SPE to carry multiple payloads mapped into STS-1 or STS-Mc (M < N) SPEs, then the necessary additional criteria will be added to this section.[2]

Note that Section 3.2.3 contains criteria related to the structure of STS-Nc SPEs, Section 3.4.3 describes the mappings of Super Rate payloads into STS-Nc SPEs, and Section 3.5.1.4 describes the use of STS Payload Pointers to identify the STS-1s that make up an STS-Nc.

5.1.3 Scrambling

SONET optical interface signals use binary line coding, and therefore must be scrambled to assure an adequate number of transitions (zeros to ones, and ones to zeros) for such purposes as line rate clock recovery at the receiver. SONET electrical interface signals use line codes that assure adequate transitions (i.e., B3ZS and CMI, see Section 4.4); however, they are also scrambled for consistency between the electrical and optical interfaces. In both cases, the scrambler used is a frame synchronous scrambler that can be applied identically at the transmitter and the receiver.

R5-6 **[134]** SONET interface signals shall be scrambled (i.e., scrambled at the transmitter and descrambled at the receiver) using a frame synchronous scrambler of sequence length 127, operating at the line rate.

... The generating polynomial for the scrambler shall be $1+x^6+x^7$.

... The scrambler shall be reset to '1111111' on the most-significant bit of the byte following the Z0 byte in the Nth STS-1 (i.e., the byte following the last Z0 byte). That bit and all subsequent bits to be scrambled shall be added, modulo 2, to the output from the x^7 position of the scrambler, as shown in Figure 5-3. The scrambler shall run continuously from that bit on throughout the remainder of the STS-N frame.

2. Such a use has been defined in SDH, but no equivalent use is defined in SONET. In the SDH case, a single Virtual Container-4 (VC-4, the SDH equivalent to an STS-3c SPE) is used to transport three independent Tributary Unit Group-3s (TUG-3s). Each TUG-3 is equivalent to an STS-1 SPE with the fixed stuff columns removed and a new column containing a payload pointer added. This additional pointer is used to identify the start of the VC-3, which in turn can contain (for example) an asynchronously mapped DS3 signal.

number as the received K1), and to inform the other end of the provisioned architecture and mode of operation.

5.4 Network Synchronization

SONET uses the existing synchronization network as described in GR-436-CORE and ANSI T1.101. This section discusses applications with respect to SONET NEs and service provider synchronization networks, timing modes for SONET NEs, criteria for SONET NE internal clocks, criteria for SONET-based timing distribution, timing reference switching criteria, and criteria regarding the use of synchronization status messages. This section also indicates which of the criteria in GR-1244-CORE are applicable to SONET NEs.

Note that in this section "OC-N" and "STS-N electrical" are generally used to identify the high-speed SONET "interfaces"[16] to a particular NE, and "OC-M" and "STS-M electrical" are used to identify any tributary SONET "interfaces". For example, in Figure 5-9 the ADM's OC-12 "interfaces" are OC-N "interfaces" and its OC-3 "interfaces" are OC-M "interfaces".

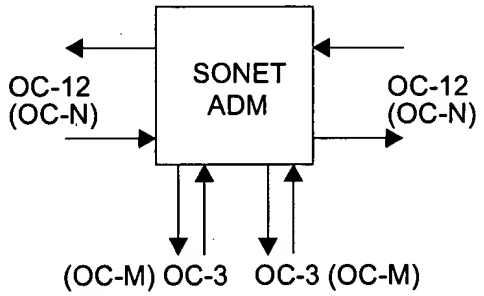

Figure 5-9. OC-N and OC-M Example

16. Throughout Section 5.4, an OC-N (or OC-M) "interface" is defined to include all of the OC-N (or OC-M) signals that are part of a "line APS" system (if supported). In turn, line APS is used to refer to protection switching architectures where an NE receives two or more OC-N (or OC-M) signals from a peer NE, and one of those signals is used to provide SONET Line layer protection for the working channel(s) carried on the other signal(s). This includes systems that support linear APS (see Section 5.3), and span-switching in 4-fiber bidirectional line switched rings (see GR-1230-CORE). If no line APS is supported for a particular pair of OC-N or OC-M signals (e.g., for the OC-N signals that connect two adjacent nodes in a UPSR), then the "interface" includes only those two (i.e., one incoming and one outgoing) signals. In this section, quotation marks will be used to distinguish between an "interface" as defined here and other types of interfaces that are commonly defined (e.g., a point in the transmission medium at which the physical layer characteristics of a signal are specified and measured).

5.4.1 SONET NE Clock Applications

In general, SONET NEs are required to have internal clocks of ±20-ppm minimum free-run accuracy. Based on the work done in T1X1 on ANSI T1.105.09, *SONET: Network Element Timing and Synchronization*, clocks that are contained in NEs that support SONET Line terminating functions, and that meet only this minimum accuracy requirement are called SONET Minimum Clocks (SMCs).

Many synchronization-related criteria are application-specific, particularly for SONET ADMs. External or loop-timing may be appropriate for a TM,[17] while external, line, or through-timing may be appropriate for an ADM. Protection switching schemes and dropped OC-M and STS-M electrical signals further complicate the selection of synchronization options. In general, most of the information and criteria applicable to a SONET ADM appear in this document; however, GR-496-CORE also contains several criteria related to the timing options that should be supported. Also note that other NEs, such as DCSs and SONET regenerators, have specific synchronization criteria that are covered in the NE-specific GRs, TRs and TAs.

The following general statements describe conditions necessary for synchronization and SONET networks to be compatible:

- Where BITS timing is available (see GR-436-CORE), SONET NEs are externally timed from the BITS clock
- Where no BITS timing is available, SONET NEs are timed from a received OC-N (or OC-M) signal
- External-timing references to a SONET NE are from a BITS clock of stratum 3 or better quality
- Timing signals delivered to the synchronization network from a SONET NE are derived directly from a terminating OC-N (or OC-M)
- Stratum 3E or 2 clocks are used between non-SONET timing distribution networks[18] and any SONET NEs containing SMC or stratum 3 clocks that require timing that is traceable from or through those networks.

5.4.1.1 Physical Interface to Synchronization Network

The physical interface for synchronization signals is important so that SONET NEs can be easily integrated into the BITS plan. BITS clocks provide two types of timing outputs. These are DS1 and Composite Clock (CC) outputs, both of which are

17. In this section, ADMs in the terminal configuration are referred to as TMs (Terminal Multiplexers), while ADMs in the add-drop configuration are simply referred to as ADMs.

18. "Non-SONET synchronization distribution network" is used here to refer to a synchronization network where a timing reference signal may contain a significantly higher amplitude of wander than allowed by Figures 5-15 and 5-16 of this document (i.e., wander corresponding to the wander tolerance TDEV mask in GR-1244-CORE).